

**REMARKS**

Claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34 are pending, and claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34 stand rejected. The applicant respectively traverses the rejection and request allowance of claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34.

Claims 1 – 4, 6 – 9, 12, 13, 18 – 21, 23 – 26, and 30 are rejected under 35 U.S.C 103(a) as being anticipated by Yu et. al. (US 6,504,846) in view of Koufopaviou (US 5493652).

Claim 1 requires:

1. An integrated circuit that processes communication packets, the integrated circuit comprising:
  - a core processor configured to create a plurality of external buffers that are external to the integrated circuit and configured to store the communication packets where each external buffers is associated with a pointer that corresponds to the external buffer;
  - a pointer cache configured to store the pointers that correspond to the external buffers;
  - control logic configured to allocate the external buffers as the corresponding pointers are read from the pointer cache and de-allocate the external buffers as the corresponding pointers are written back to the pointer cache wherein the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold; and
  - the core processor configured to create additional external buffers and their corresponding pointers in response to the exhaustion signal.

Claim 1 has the limitation that “the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a

minimum threshold". The examiner states that Yu does not disclose transferring an exhaustion signal if the number of the pointers to the de-allocated buffers reaches a minimum threshold. The examiner cites column 3 lines 15 – 20, and column 4 lines 20 – 46 of Koufopaviou as teaching transferring of an exhaustion signal when the number of pointers to the de-allocated buffers reaches a minimum. The examiner has mischaracterized the cited art. Koufopaviou does not have an exhaustion signal that is activated when the number of pointers in a buffer falls below a threshold. The cited art talks about a buffer that contains pointers, but the number of pointers in the buffer is not compared to a threshold.

Furthermore, in Koufopaviou, even when the number of pointers in the buffer reach zero nothing happens. In fact the main idea in Koufopaviou is to reduce the number of pointers in the buffer to zero, indicating that there are no empty buffers mixed in with the full buffers (i.e. all the empty buffers are in the contiguous empty buffer section). The current invention is completely different in that the object is to maintain at least a minimum number of pointers in the buffer.

In addition, Koufopaviou does not create additional buffers and their corresponding pointers. Koufopaviou has a fixed number of buffers.

Because Yu and Koufopaviou do not contain a core processor that creates additional buffers in response to the exhaustion signal, as required by claim 1, the examiner has not established the requirements for a *prima facie* case of obviousness. Therefore Claim 1 is allowable as written.

Claims 2 – 4 and 6 – 17 depend on allowable claim 1. Therefore claims 2 – 4 and 6 – 17 are also allowable.

Claim 18 also has a limitation that additional buffers are created in response to the exhaustion signal. Therefore the arguments for claim 1 (above) apply to claim 18 and claim 18 is allowable as written.

Claims 19 - 21 and 23 - 28 and 30 - 34 depend on allowable claim 18. Therefore claims 19 - 21 and 23 - 28 and 30 - 34 are also allowable.

The prior art made of record and not relied upon has been reviewed and is not considered relevant.

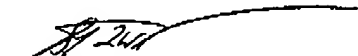
#### Conclusion

Based on the above remarks, the Applicants submit that claims 1 - 4, 6 - 21, 23 - 28 and 30 - 34 are allowable. There may be additional reasons in support of patentability, but such reasons are omitted in the interests of brevity. The Applicants respectfully request allowance of 1 - 4, 6 - 21, 23 - 28 and 30 - 34.

Any fees may be charged to deposit account 502622.

Respectfully submitted,

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